N-Channel Enhancement Mode MOSFET

TBL120N10T-5DL8

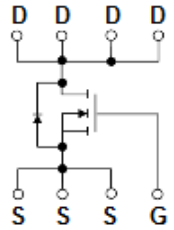
Features

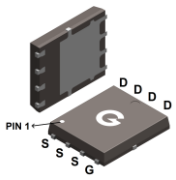
- Advanced shielded-gate trench technology
- Super low R_{DS}(on) and gate charge
- Green device available
- HBM: AEC-Q101-001: H1A (JESD22-A114-B: 1A)
- RoHS compliant with Halogen-free
- Qualified to AEC-Q101 Standards

HF

Mechanical Data

- Case: PDFN5×6-8L
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208





PDFN5×6-8L

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
TBL120N10T-5DL8	PDFN5×6-8L	5000 pcs / Tape & Reel	120N10T

Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	100	V
Gate-to-Source Voltage	V_{GSS}	±20	V
Continuous Drain Current (T_C = 25°C)	I_D	57	A
Continuous Drain Current (T_C = 100°C)		40	
Continuous Drain Current (T_A = 25°C) *1		11	
Continuous Drain Current (T_A = 100°C) *1		7.8	
Pulsed Drain Current (t_p =10μs, T_C = 25°C)	I_{DM}	243	A
Single Pulse Avalanche Energy (L = 0.5mH) *3	E_{AS}	27	mJ
Single Pulse Avalanche Energy (L = 0.1mH)		13	
Power Dissipation (T_C = 25°C)	P_D	79	W
Operating Junction Temperature Range	T_J	-55 ~ +175	°C
Storage Temperature Range	T_{STG}	-55 ~ +175	°C

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	-	1.4	1.9	°C/W
Thermal Resistance Junction-to-Air *1	$R_{\theta JA}$	-	35	50	°C/W

Electrical Characteristics (@ T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics						
$R_{DS(ON)}$	Drain-Source On-resistance *2	V_{GS} = 10V,I_D = 20A	-	10.5	12	mΩ
		V_{GS} = 4.5V,I_D = 20A	-	15	17	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.8	2.6	V
R_G	Gate Resistance	V_{GS} = 0V, f = 1MHz	-	5.7	-	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V V_{DS} = 50V f = 150KHz	-	1800	-	pF
C_{OSS}	Output Capacitance		-	550	-	
C_{RSS}	Reverse Transfer Capacitance		-	22	-	
Switching Characteristics						
$t_{d(ON)}$	Turn-on Delay Time *4	V_{DD} = 50V V_{GS} = 15V R_G = 3.3Ω I_D = 20A	-	10	-	ns
t_r	Turn-on Rise Time *4		-	58	-	
$t_{d(OFF)}$	Turn-Off Delay Time *4		-	45	-	
t_f	Turn-Off Fall Time *4		-	11	-	
di/dt(on)	di/dt(on) Ruggedness		-	366	-	A/μs
dv/dt(on)	dv/dt(on) Ruggedness		-	0.65	-	V/ns
di/dt(off)	di/dt(off) Ruggedness		-	480	-	A/μs
dv/dt(off)	dv/dt(off) Ruggedness		-	3	-	V/ns
Q_G	Total Gate-Charge	V_{DD} = 50V V_{GS} = 10V I_D = 20A	-	31	-	nC
Q_{GS}	Gate to Source Charge		-	6.1	-	
Q_{GD}	Gate to Drain (Miller) Charge		-	6.9	-	
Source-Drain Diode Characteristics						
V_{SD}	Diode Forward Voltage *2	I_{SD} = 20A, V_{GS} = 0V	-	0.9	1.2	V
trr	Reverse Recovery Time	I_F = 20A, V_{GS} = 0V di/dt = 100A/μs	-	47	-	ns
Qrr	Reverse Recovery Charge		-	63	-	nC

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper
2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%
3. The E_{AS} data shows Max. rating. The test condition is V_{DD} = 50V, V_{GS} = 10V, L = 0.5mH
4. Guaranteed by design, not subject to production

Ratings and Characteristics Curves (@ T_A = 25°C unless otherwise specified)

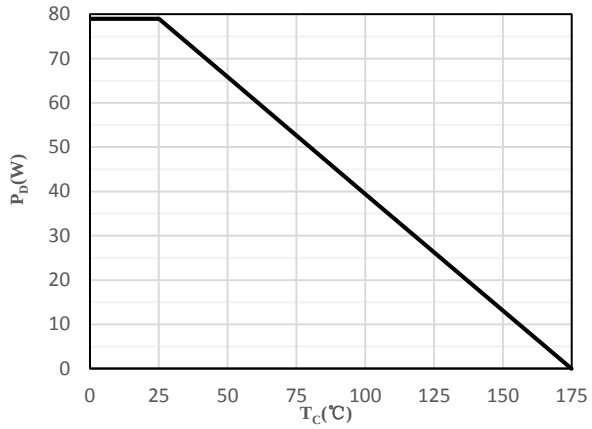


Fig 1 Power Dissipation

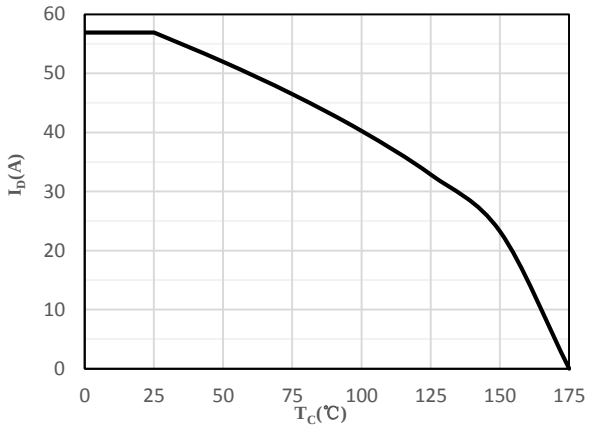


Fig 2 Drain Current

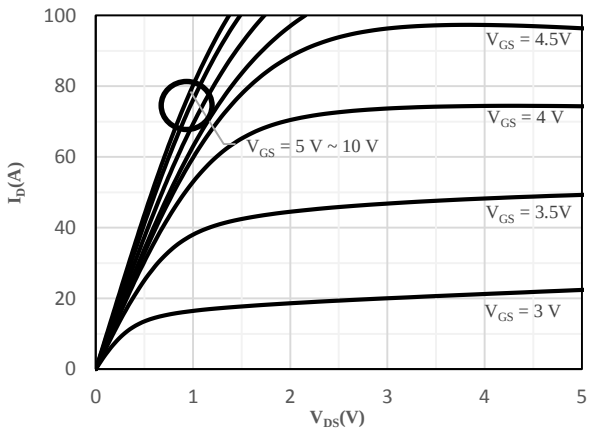


Fig 3 Typical Output Characteristics

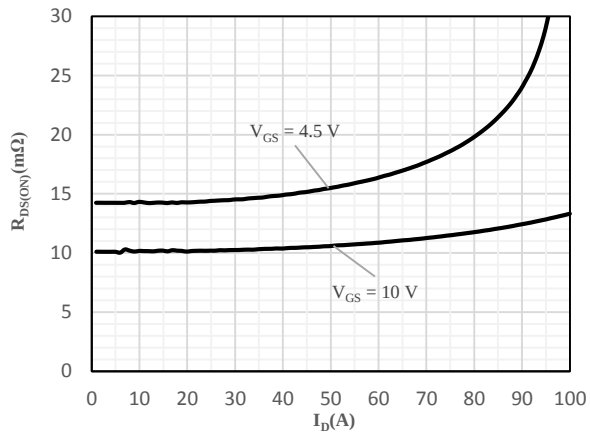


Fig 4 On-Resistance vs. Drain Current and Gate Voltage

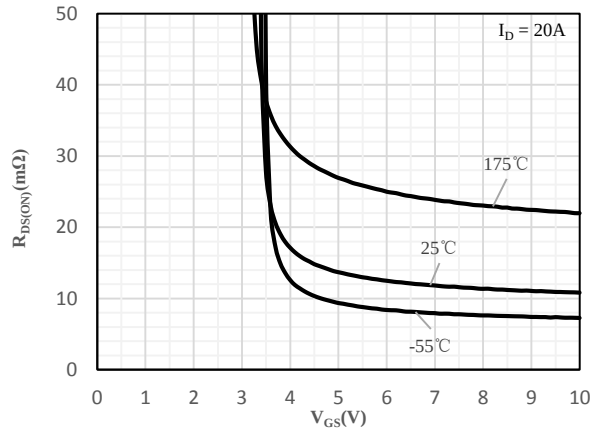


Fig 5 On-Resistance vs. Gate-Source Voltage

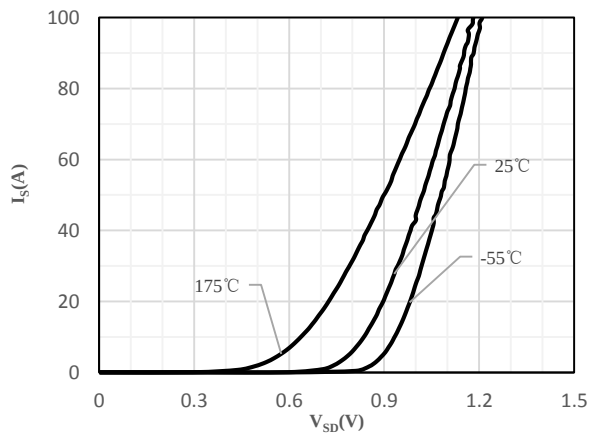


Fig 6 Body-Diode Characteristics

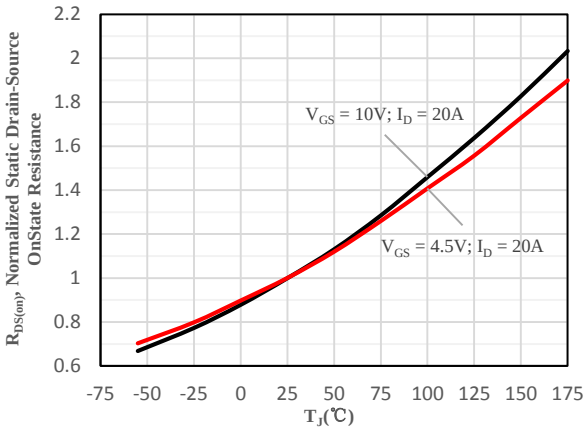


Fig 7 Normalized On-Resistance vs. Junction Temperature

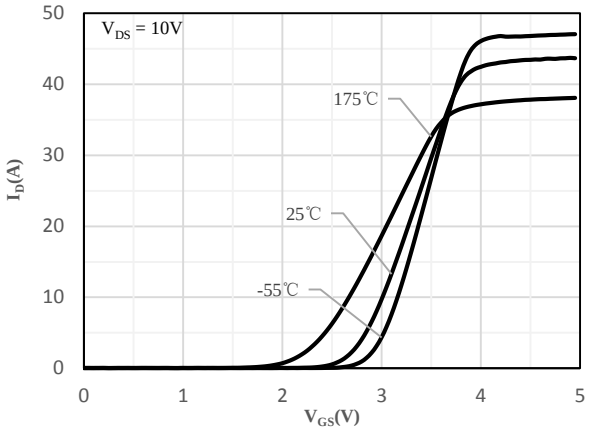


Fig 8 Transfer Characteristics

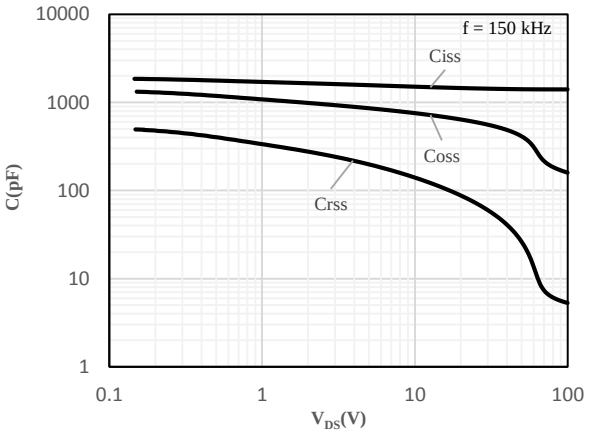


Fig 9 Capacitance Characteristics

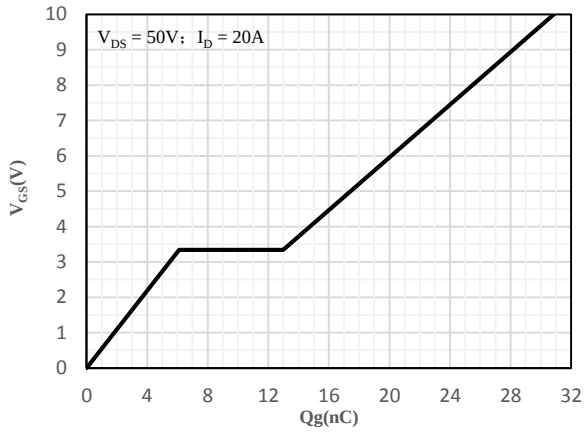


Fig 10 Gate-Charge Characteristics

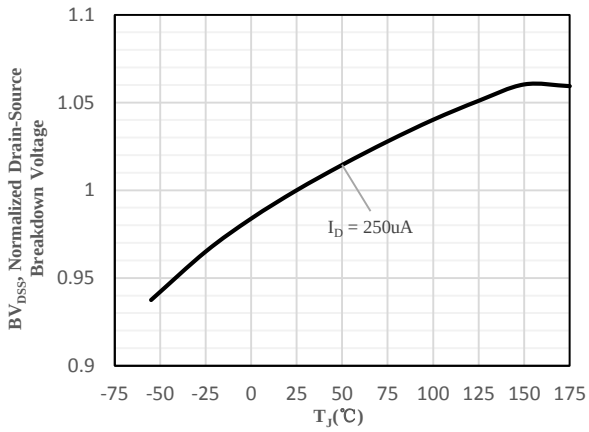


Fig 11 Normalized Breakdown Voltage vs. Junction Temperature

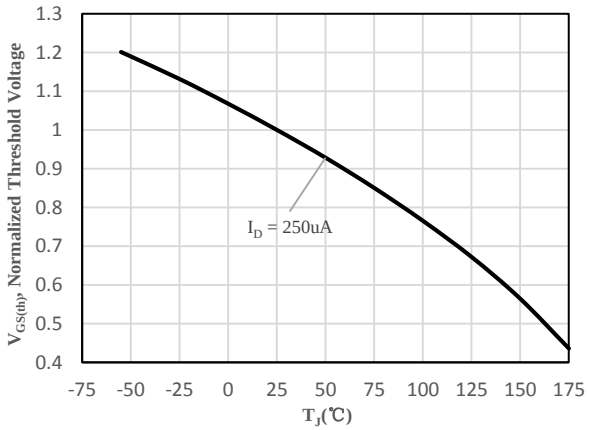


Fig 12 Normalized $V_{GS(th)}$ vs. Junction Temperature

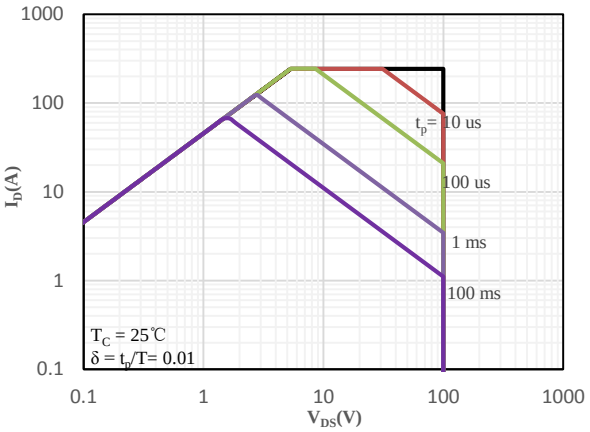


Fig 13 Safe Operating Area

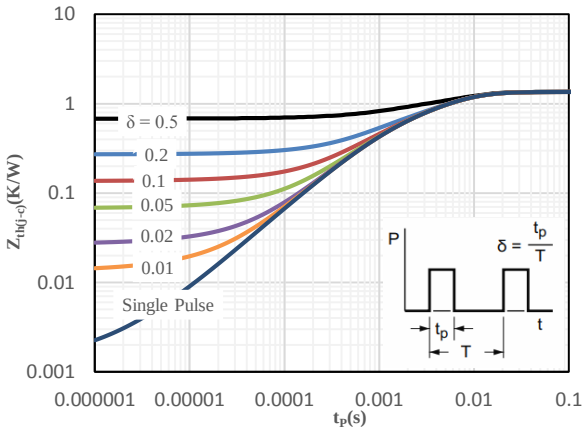
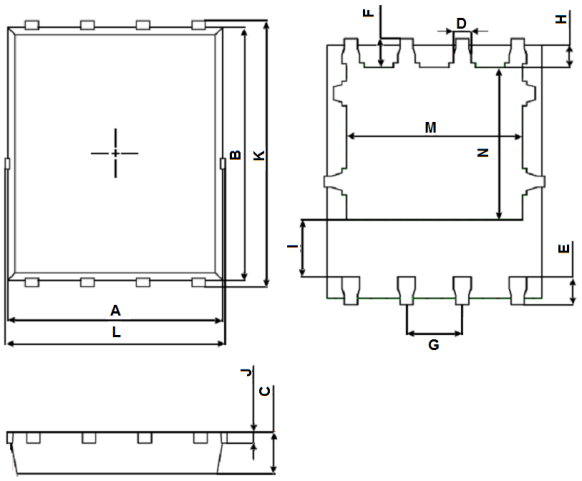


Fig 14 Maximum transient thermal impedance

Package Outline Dimensions (Unit: mm)



PDFN5×6-8L		
Dimension	**Min.**	**Max.**
A	4.824	4.976
B	5.674	5.826
C	0.900	1.000
D	0.350	0.450
E	0.559	0.711
F	0.574	0.726
G	1.250	1.290
H	0.424	0.576
I	1.190	1.390
J	0.154	0.354
K	5.974	6.126
L	4.944	5.096
M	3.910	4.110
N	3.375	3.575

Mounting Pad Layout (Unit: mm)

PDFN5×6-8L